CLAIMS:

1. A wafer (1), which wafer (1) comprises a number of exposure fields (2) and which wafer (1) comprises a number of lattice fields (3) in each exposure field (2), wherein each lattice field (3) contains an IC (4), and which wafer (1) comprises a first group (5) of first dicing paths (6) and a second group (7) of second dicing paths (8), wherein all of the first dicing paths (6) of the first group (5) run parallel to a first direction (X) and have a first path width (W1) and wherein all of the second dicing paths (8) of the second group (7) run parallel to a second direction (Y) intersecting the first direction (X) and have a second path width (W2), and wherein the first dicing paths (6) and the second dicing paths (8) are provided and designed for a subsequent segregation of the lattice fields (3) and the ICs (4) contained therein, and wherein in each exposure field (2) at least two control module fields (A1, A2, A3, A4, B1, B2, B3, B4, C2, C4, D2, D4, E1, E3, F1, F3, G2, H1, J1) are provided, each of which control module fields (A1, A2, A3, A4, B1, B2, B3, B4, C2, C4, D2, D4, E1, E3, F1, F3, G2, H1, J1) contains at least one optical control module (OCM-A1, OCM-A2, OCM-A3, OCM-A4, OCM-B1, OCM-B2, OCM-B3, OCM-B4, OCM-C2, OCM-D4), and wherein each control module field (A1, A2, A3, A4, B1, B2, B3, B4, C2, C4, D2, D4, E1, E3, F1, F3, G2, H1, J1) provided in an exposure field (2) is provided in place of a preset number of lattice fields (3), and wherein the at least two control module fields (A1, A2, A3, A4, B1, B2, B3, B4, C2, C4, D2, D4, E1, E3, F1, F3, G2, H1, J1) of each exposure field (3) are arranged at an average distance (K) from one another extending in the second direction (Y), which average distance (K) is equal to at least a quarter of the side length (L) of a side (M) of the exposure field (2) which extends in the second direction (Y).

2. A wafer (1) as claimed in claim 1, wherein the average distance (K) is equal to the whole side length (L) of a side (M) of the exposure field (2) which extends in the second direction (Y) minus the side length (N) of a side (P) of a lattice field (3) which extends in the second direction (Y).

3. A wafer (1) as claimed in claim 1, wherein each exposure field (2) is designed rectangular, and wherein four control module fields (A1, A2, A3, A4, B1, B2, B3, B4, C2,

C4, D2, D4, E1, E3, F1, F3, G2, H1, J1) are provided in each exposure field (2), and wherein each control module field (A1, A2, A3, A4, B1, B2, B3, B4, C2, C4, D2, D4, E1, E3, F1, F3, G2, H1, J1) is located in a corner region of the exposure field (2) in question.

4. A wafer (1) as claimed in claim 1, wherein each control module field (A1, A2, A3, A4, B1, B2, B3, B4, C2, C4, D2, D4, E1, E3, F1, F3, G2, H1, J1) provided in an exposure field (2) is provided in place of one lattice field (3) only.